ABSTRACT

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The present invention concerns a method for the functional verification of a software model (40) of an integrated circuit on demand (ASIC), in a low-level language (for example of the HDL type), which separately handles the creation of the model and the debugging of the functional verification tests to be applied to the model of the circuit in order to create a verification platform, comprising the following two steps:

- creation of an autonomous circuit emulator (1), obtained by replacing the model in a low level (HDL-type) language physically describing the circuit under design to be validated with a high level (for example C++) abstract description generating response data structures in accordance with the functional specification (20) of the design as a function of the stimuli received, this mode being called the "transmission mode";

- integration of the software model (40) in low level (HDL-type) language of the circuit resulting from the design into a verification platform, and creation of the connection of the previously validated autonomous circuit emulator (1), in parallel, to the interfaces of the software model (40) of the circuit, and of the connection of an environment emulator (11, 21, 22); and

- utilization of this platform as a reference for the validation of the response data trnasmitted by the software model (40) of the circuit, this mode being called the "verification mode."

Figure 1